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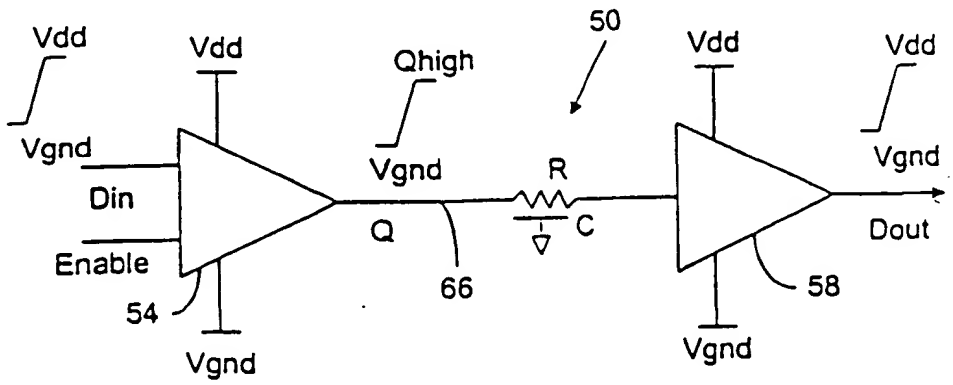

(57) Abstract

In some embodiments, the invention includes an interconnect system (50) having a single ended driver (54) and single ended hysteretic receiver (58). A single ended interconnect (66) is coupled between the single ended driver and single ended receiver. In other embodiments (figure 4), the invention involves an interconnect system including interconnects (66A, 66B), single ended drivers (54A, 54B), and single ended hysteretic receivers (58A, 58B) connected to respective ones of the interconnects. The single ended drivers receive respective data-in signals (Din(0), Din(1)) and an enable signal (Enable) and wherein the drivers transmit interconnect signals on the interconnects when the enable signal is asserted. In yet other embodiments (140), the invention includes an interconnect system having interconnects (66A, 66B), quasi-static drivers (142A, 142B) and receivers (150A, 150B) connected to respective ones of the interconnects, the quasi-static drivers receive a clock signal (CLK) and respective data-in signals (Din(0), Din(1)), and wherein the interconnect signals are pre-discharged when the clock signal changes from a first to a second state, and wherein when the clock signal is in the first state, the interconnect signals are related to the data-in signals. In still other embodiments, the invention includes a pseudo differential interconnect system (90) and an interconnect system with a dual rail driver (190).

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SINGLE ENDED INTERCONNECT SYSTEMS

Background of the Invention

Technical Field of the Invention: The present invention relates to interconnect systems including a driver, interconnect, and receiver.

Background Art: Point-to-point on-chip interconnects between and within Functional Unit Blocks (FUBs) in semiconductor chips have evolved with integration as major on-chip performance and power bottlenecks. This is primarily because interconnect capacitance per unit length, dominated by sidewall fringing and cross-coupling, may increase hyperbolically with lateral dimension scaling and hence scale slower than does gate capacitance.

Mixed voltage swing based techniques have been studied for high performance/low power on-chip datapath interconnects. In mixed voltage swings techniques, the interconnects are driven at a reduced voltage swing, offering significant dynamic power and driver delay reduction. Mixed-swing techniques include those involving fully-differential interconnects. For example, Fig. 1 illustrates an interconnect system 10 including a driver 12 and a receiver 14. A single ended digital signal X having a swing between Vgnd and Vdd1 is received by driver 12. Signal X is converted by driver 12 into reduced swing signals Y and Y* on interconnects 20A and 20B (where Y* is the complement of Y). The resistance and capacitance of the interconnect is represented schematically by a resistor R and a capacitor C. Both signals Y and Y* have a swing of between Vgnd and Vdd2, where Vdd2 < Vdd1. Signals Y and Y* are received by receiver 14 and converted therein back to a single ended signal Z have a full swing of between Vgnd and Vdd1 and which follows signal X or is its complement. Some prior art interconnect systems include an enable signal.

Noise immunity would be decreased by lowering the signal swing, however, the fully-differential interconnect technique helps improve noise immunity through common mode noise rejection. Further, fully differential receivers can avoid static power consumption during swing restoration. However. such approaches entail

approximately a 2X penalty in interconnect layout area and effective switched capacitance per cycle due to their fully differential nature. Therefore, power reduction achieved due to the reduced swing is offset by the power penalty paid in driving the 2X high switched capacitance.

Accordingly, there is a need for an interconnect system that reduces power consumption and/or interconnect area.

Summary

In some embodiments, the invention includes an interconnect system having a single ended driver and a single ended hysteretic receiver. A single ended interconnect is coupled between the single ended driver and single ended receiver.

In other embodiments, the invention involves an interconnect system including interconnects, single ended drivers, and single ended hysteretic receivers connected to respective ones of the interconnects. The single ended drivers receive respective data-in signals and an enable signal and wherein the drivers transmit interconnect signals on the interconnects when the enable signal is asserted.

In yet other embodiments, the invention includes an interconnect system having interconnects, quasi-static drivers and receivers connected to respective ones of the interconnects. The quasi-static drivers to transmit interconnect signals on the interconnects, the quasi-static drivers receiver a clock signal and respective data-in signals, and wherein the interconnect signals are pre-discharge when the clock signal changes from a first to a second state, and wherein when the clock signal is in the first state, the interconnect signals are related to the data-in signals.

In still other embodiments, the invention includes a pseudo differential interconnect system and an interconnect system with a dual rail driver.

Brief Description of the Drawings

The invention will be understood more fully from the detailed description given below and from the accompanying drawings of embodiments of the invention which, however, should not be taken to limit the invention to the specific embodiments described, but are for explanation and understanding only.

FIG. 16 illustrates a driver 250 without tri-state capability (e.g., that could be used in FIG. 3). Driver 250 includes nFET transistors M41 and M42 and inverters 252 and 254.

Although the illustrated embodiments include enhancement mode transistors, depletion mode transistors could be used in place of some or all the transistors.

It is not necessarily required that Vdd of the driver equal Vdd of the receiver.

Examples of hysteretic circuits are described herein in connection with FIGS. 11 and 12. Although the circuits in FIGS. 11 and 12 are presented as receivers for interconnect signals, the circuits may be used in various other contexts such as an output stage for a reduced voltage domino circuit.

There may be intermediate structure (such as a buffer or driver to increase the voltage of a signal) between two illustrated structures or within a structure (such as a circuit or conductor) that is illustrated as being continuous. The borders of the boxes in the figures are for illustrative purposes and not intended to be restrictive. Arrows show certain signal flow in certain embodiments, but not every signal, such as control signals and requests for data.

If the specification states a component, feature, structure, or characteristic "may", "might", or "could" be included, that particular component, feature, structure, or characteristic is not required to be included. Reference in the specification to "some embodiments" means that a particular feature, structure, or characteristic described in connection with the embodiments is included in at least some embodiments, but not necessarily all embodiments, of the invention. The various appearances "some embodiments" are not necessarily all referring to the same embodiments.

Those skilled in the art having the benefit of this disclosure will appreciate that many other variations from the foregoing description and drawings may be made within the scope of the present invention. Accordingly, it is the following claims including any amendments thereto that define the scope of the invention.

CLAIMS

What is claimed is:

1. An interconnect system comprising:

a single ended driver;

a single ended hysteretic receiver; and

a single ended interconnect coupled between the single ended driver and single ended receiver.

2. The system of claim 1, wherein the single ended driver is a first driver and the single ended hysteretic receiver is a first reviver and wherein the system is a bidirectional signaling interconnect system including a second single ended driver and a second single ended hysteretic receiver coupled to the interconnect, and wherein the second driver transmits an interconnect signal on the interconnect to the second receiver in an opposite direction than the first driver transmits an interconnect signal to the first receiver.

3. The system of claim 1, wherein the receiver includes pull up transistors cross-coupled between nodes and a transistor connected to one of the nodes that accelerates the fall of one of the nodes and after a low to high transition of an input signal, holds the node to a low voltage unless the input signal goes below a reverse trip point which is lower than a forward trip point.

4. The system of claim 1, wherein the receiver includes a riding transistor involving no static power consumption.

5. The system of claim 1, wherein the driver includes an nFET source follower device that pull ups an interconnect signal to a first voltage value and a p-booster pFET device pulls the interconnect signal to a power supply voltage.

6. The system of claim 4, wherein an inverter is connected between the gate of the nFET device and the gate of the pFET device.

7. The system of claim 1, wherein the driver transmits an interconnect signal that has a high voltage equal to a power supply voltage minus a threshold voltage of an nFET device and wherein the system further includes body bias voltage circuitry to control the threshold voltage of the nFET device.

Vdd - Vt. This offers substantially improved receiver power supply noise rejection as compared to conventional static CMOS receiver.

If noise on signal Q pulls signal Q below VTP2, M21 will be partially turned OFF. Further, node N1 will be lowed somewhat through device MR, which will begin to turn ON. However, if Q does not go below VRP1, node N1 will continue to keep Mhys ON enough to keep node N2 low and node N1 will not be low enough to sufficiently turn ON M23 to pull up node N2. If signal Q goes below VTP1, M21 will turn substantially OFF, MR will turn ON sufficiently to pull node N1 low, which will turn OFF Mhys. Further, with node N1 low, M23 will turn on, pulling up node N2 and turning ON M22.

Both receivers 170 and 190 are static. Therefore, receiver dynamic power consumption drops linearly with reducing bus switching activity, i.e., the receiver load capacitance is switched only when input data transitions, else the state is retained. This represents a substantial savings in power compared to other dynamic prior art receiver approaches, because such schemes precharge and evaluate the receiver outputs every cycle independent of input data activity, contributing to a large dynamic power loss at low input data activities.

In receivers 170 and 190, power and ground rails (Vdd and Vgnd) may be shared with peripheral circuitry operating at CMOS levels, so that additional power rails are not necessary.

Since receivers 170 and 190 have only a single-ended input, transmitting the complementary signal (as in prior art fully-differential approaches) is not required. This eliminates the power consumed in driving the complementary interconnect as well as the driver and interconnect layout area associated with transmitting the complementary signal.

2. A Receiver for Quasi-Static Drivers

Referring to FIG. 15, receiver 240 is an example of receivers 150A and 150B of quasi static interconnect system 140 in FIG. 9. Receiver 240 includes pFET transistors M30 and M31 and nFET device M32. Receiver 240 is insensitive to a high to low transition when the Q signal is pre-discharged because the clock is high so that M30 is OFF. When Clk is low, Dout is the inverse (complement) of interconnect signal Q.

When Q is low and Clk is high, output conductor 244 is in a high impedance tri-state condition and retains its previous state.

D. Bidirectional Signaling

In the case of tri-stated drivers, such as driver 100, multiple drivers can drive the same bus (with only one driver's tri-state enable signal asserted during a given clock phase). Bidirectional signaling may occur on the interconnects by controlling timing of the signaling and the enable signals. This has the potential to offer a full 2X or more improvement in bandwidth compared to a uni-directional repeater-based transceiver circuit.

For example, referring to FIG. 17, in an interconnect system 260, data is transmitted in opposite directions on interconnect 66. System 260 includes single ended drivers 264A and 264B receiving enable signals and single ended receivers 266A and 266B. Examples of drivers 264A and 264B include drivers 100, 120, or 130 in FIGS. 6 - 8. At certain times, driver 264A is enabled and driver 264B is not and vice versa. For example, in some embodiments, during a first half phase of a clock cycle, driver 264A is enabled and driver 264B is not enabled, so that the output of driver 264B is in a high impedance state. During the second half phase of the clock cycle, driver 264B is enabled and driver 264A is not enabled, so that the output of driver 264A is in a high impedance state. (There may be more than two drivers participating in signaling over interconnect 66. In such a case, a clock cycle might be divided into more than two phases.)

There are at least three possible receiver arrangements. Under a first scheme, each receiver is allowed to switch regardless of which driver is driving interconnect 66. However, the output of receiver 266B may be ignored during the phase in which driver 264A is driving a signal on interconnect 66. Likewise, the output of receiver 266A may be ignored during the phase in which driver 264B is driving a signal on interconnect 66. Under a second scheme, illustrated in FIG. 18, the receivers receive enable signals and are allowed to switch only when enabled. Under a third scheme, illustrated in FIG. 19, the receivers do not receive enable signals but logic (e.g., logic 270) at the output of the receives does.

E. Other Information and Embodiments

nFET device Mhys (for hysteresis) is OFF, a pFET device M11 is ON pulling node N2 high turning OFF a pFET device M12. PFET devices M11 and M12, which are cross-coupled together, and nFET devices M13 and M14, which receive signals Q and Q*, look similar to a cascode voltage switched gate. However, they differ from a cascode voltage switched gate because of the inclusion of nFET device Mhys.

When Q is changed from Vgnd (low) to Vdd - Vt, which is greater than VTP2, M13 turns ON, pulling down node N2, which turns M12 ON. With M12 ON, node N1 is pulled up. Contention between M12 and M14 is quickly resolved because with Q being high, M15 and M16 turn OFF, and M17 turns ON pulling Q* low. With Q* low, M14 turns OFF. As node N1 is pulled high, transistor M11 is turned OFF and transistor Mhys is turned ON to accelerate the fall of node N2. Accordingly, transistor M12 is turned on stronger as transistor M14 is turned OFF.

The nFET device Mhys contributes to the hysteretic receiver 170 as follows. When Mhys is at ground, it acts as a drain follower device (i.e., the drain follows the inverse of the input Q) with the gate tied to Vdd. Node N2 is pinned to Vgnd by Mhys. If Q goes below the trip point VTP2 because of noise, M13 starts to turn OFF, but transistor Mhys will continue to be ON keeping node N2 low and M12 ON. M15 and M16 may turn partially ON and M17 may turn partially OFF so that Q* is higher such that M14 may turn partially ON. There may be some contention between M12 and M14, but not enough to pull node N1 low and completely turn Mhys OFF. However, if Q is pulled low, below VTP1, M13 will turn OFF, Q* will be pulled high turning M14 ON, which will pull node N1 low and turn OFF Mhys and turn ON M11. With node N2 high, M12 turns OFF. Generally speaking, the reverse trip point VTP1 is the point at which these other effects of receiver 170 can overcome the hysteretic effect of Mhys. By properly sizing devices Mhys and parameters such as the size of M11, M12 and perhaps M14, a proper reverse trip point VTP1 may be selected and the desired noise immunity be provided. As well as significantly contributing to the hysteresis, Mhys increases the speed at which node N2 is pulled down, adding to the overall speed (and decreasing the delay) of receiver 170.

In the case in which Q is Vdd - Vt, M17 will be ON, but M15 and M16 might not be completely OFF. Accordingly, there may be a small amount of static current

through M15 and M16. By stacking M15 and M16, that amount of static current is significantly reduced. The stack of M15 and M16 also reduces leakage current which helps with noise immunity. When a device is leaky, it may act like a biased amplifier and tend to be near a precipice of switching.

b. A Second Hysteretic Receiver

Referring to FIG. 12, a hysteretic receiver 190 has a forward trip point VTP2, which is greater than a reverse trip point VTP1, similar to that shown in FIG. 13. Receiver 190 includes nodes N1 and N2. As illustrated, receiver 190 includes an inverter 194. An output signal Dout (having a voltage Vout) is provided the output of inverter 194. To the extent a signal Dout* (the complement of Dout) is desired, it can be obtained at node N2 or at the output of another inverter (not shown) in series with inverter 190. Dout may be at node N1. It is assumed Q is a low voltage swing signal where Qhigh is Vdd - Vt absent noise, but receiver 190 will provide hysteresis and the description is largely applicable if Qhigh is Vdd or some other high value absent noise.

As explained above, in receiver 170, static power is reduced, but not eliminated. In receiver 190, the static power is eliminated. Assuming signal Q switches from 0 to Vdd - Vt, when Q is high, nFET device M21 turns ON and pulls node N2 low, turning on a pFET device M22. When M22 is ON, a node N1 goes high, which turns a pFET device M23 OFF. With node N1 high, an nFET device Mhys is turned ON accelerating the fall of node N2. Accordingly, Mhys increases the speed at which Dout switches to high. An nFET device MR (called a riding device) has its gate tied to Vdd. MR is ON when Q is low, because Vgs is roughly Vdd. However, as Q goes from 0 to Vdd - Vt, Vgs is Vdd - (Vdd - Vt) = Vt, which roughly the Vt of MR. (It is assumed that the Vts of the transistors is roughly equal to the Vt of the driver, although that is not required.) Accordingly, MR turns OFF. There is not a static (DC) path between power supply Vdd and ground. When Q is at Vdd - Vt, MR does see a direct path from Vdd to ground so that there is no DC current through MR. Accordingly, with receiver 190 there is hysteretic noise immunity without having a DC path from Vdd to ground.

The drain to source resistance of MR is very high when $Vgs \leq Vt$. Q is protected from power supply by the very high impedance. Accordingly, signal Q is isolated from noise on Vdd (power supply) because of high impedance when input at

switching is anti-phase. In quasi-static interconnect system 140, the interconnect signals Q on the different interconnects is pre-discharged simultaneously when Clk is high so that the Q1 and Q2 signals always start at low. The interconnect signals Q then switch depending on the Din signals when the clock goes low. This prevents anti-phase MCF.

System 140 includes receives 150A and 150B, which are representative of other receivers in the system. Although a variety of receiver designs may be used, a driver (as described below) that is insensitive to high to low transitions would be preferred for some applications.

Referring to FIG. 10, a p-boosted quasi-static driver 154 is shown which is similar to driver 142A except that it includes an inverter 156 and a pFET device M8. NFET device M5 does most of the work in pulling up interconnect signal Q. After a delay through inverter 156, pFET device M8 pulls Q to Vdd. PFET device M8 and the transistors of inverter 156 may be relatively small.

4. Dual-Rail Pseudo-Differential Driver

Referring to FIG. 14, a single ended dual rail pseudo differential driver 210 includes a NOR gate 214 and an OR gate 216 that receive a clock (Clk) signal and a Data signal. A signal A is at the output of NOR gate 214 and a signal B is at the output of OR gate 216. Driver 210 includes a source follower nFET device M25 and a p-booster pFET device M27, as well as pull down nFET devices M26 and M28. Signal A is high when both the Clk and data signals are low, but is otherwise low. Signal B is low when both the Clk and data signals are low, but is otherwise high. When the Clk signal transitions from low to high, signal Q is predischarged. Then, after the Clk signal returns to low, the signal Q is the opposite state of the Data signal. There is no contention offered by nFET device M26 to the pull-up devices M25 and M27. This lack of contention offers significant performance improvement over prior art CMOS drivers.

C. Receiver Circuits

A variety of receiver circuits may be used in connection with the single ended driver circuits.

1.

Hysteretic Receivers

Receivers 170 and 190, described below, may be used as receiver 58 in FIGS. 2 and 3.

a. A First Hysteretic Receiver

As mentioned, referring to FIGS. 2 and 3, drivers 54 and 74 drive an interconnect signal Q having a swing between Vgnd and Qhigh. Where Qhigh is less than Vdd (e.g., Vdd - Vt), the noise margin between Qhigh and Vdd/2 is relatively low. Noise that would not cause Vdd to dip below Vdd/2, may cause Vdd - Vt to dip below Vdd/2. Referring to FIG. 11, to solve this problem, a hysteretic single ended receiver 170 requires interconnect signal Q to go substantial below the forward going trip point to trip a high to low transition. Receiver 170 provides high noise immunity in a single ended interconnect system that has the performance and power savings advantage of a mixed swing technique and the interconnect density of a single ended system.

Referring to FIG. 11, in the following description, it is assumed Q is a low voltage swing signal where Qhigh is Vdd - Vt absent noise, but receiver 170 will provide hysteresis and the description is largely applicable if Qhigh is Vdd or some other high value absent noise. Receiver 170 includes an output signal Dout with a voltage Vout that follows the voltage Vin of single ended interconnect signal Q (as opposed to a differential input). It may also be desirable to have a Dout* signal, which is the complement of Dout. In FIG. 11, Dout is at node N1 and Dout* is at node N2. The voltage of Dout and Dout* could be increased by putting an inverter at nodes N1 and N2 and having Dout be at the output of the inverter on node N2 and Dout* be at the output of the inverter on node N1.

The hysteretic nature of receiver 170 is illustrated with FIG. 13 (which may be somewhat idealized) wherein a forward trip point (low to high voltage) VTP2 of Q(Vin) at which Dout switches from a low to high voltage is significantly higher than a reverse trip point VTP1 (high to low voltage) of Vin at which Dout switches from a high to a low voltage. As an example, VTP2 may be Vdd /2 (or another value).

Receiver 170 includes inverter 174, having pFET devices M15 and M16 and an nFET device M17, the output of which is a signal Q* which is the complement of Q. When Q is low, an nFET device M13 is OFF, Q* is high, M14 is ON, Dout is low, an

The high drive impedance provided by nFET device M1 when Q is at Vdd - Vt offers substantially improved driver-end power supply noise rejection when compared with conventional full-swing static CMOS approaches which use a pFET device in place of nFET device M1. This is due to the relatively high drain-source impedance of the nFET-only driver.

The threshold voltage Vt of nFET device M1 can be changed by changing the bias voltage Vbody applied to the body of M1. Referring to FIG. 7, a driver 120 is like driver 100 (in FIG. 6) except as follows. In driver 100, the bodies of devices M1, M2, and M3 are tied to Vgnd, so there is a zero bias, whereas in driver 120, the bodies of devices M1, M2, and M3 are connected to the output of body bias voltage circuitry 124. Circuit 124 provides a voltage Vbody on a conductor 128, which may be greater than Vgnd (in which case devices M1, M2, and M3 are forward biased), equal to Vgnd, or less than Vgnd (in which case devices M1, M2, and M3 are reverse biased). A forward bias of the source-drain junction reduces the driver devices' threshold voltage, contributing to further delay improvement but may increase power consumption. Conductor 128 may be connected to various places including body taps and the bottom of the substrate. Body bias voltage circuitry 124 may include feedback circuitry to keep Qhigh at a desired value or maintain another parameter(s). Devices M1, M2, and M3 may share a common body (although they may be referred to as separate bodies) or, for example, have separate bodies in different wells. If device M1 is isolated from devices M2 and M3, the body of device M1 could be connected to conductor 128 as illustrated in FIG. 7, while the body of devices M2 and M3 could be connected to Vgnd as illustrated in FIG. 6. Body bias may be applied to transistors of the other circuits illustrated and/or described herein.

2. Drivers With Full Swing

Referring to FIG. 8, driver 130 is similar to driver 100 except that driver 130 includes a pFET device M4 and an inverter 134 between the output of the gate of nFET device M1 and pFET device M4. Driver 130 is, therefore, referred to as a p-boosted driver. NFET device M1 does almost all the work in pulling Q high, but can only pull to Vdd - Vt. After the delay of inverter 134, pFET device M4 pulls Q the remainder of the way to Vdd. PFET device M4 is considerably weaker than is nFET device M1.

Advantages of a p-boosted driver include that it has a full swing, which may lead to better noise immunity if a prior art receiver is used. Further, pFET device M4 and inverter 134 may be considerably smaller than would a pFET device that does all the pulling up.

3. Quasi-Static Driver

Drivers 100, 120, and 130 are static drivers in that the interconnect signal Q toggles (changes from low to high or high to low) only when the Din signal toggles (and when the enable signal is asserted if an enable signal is included in the driver). Accordingly, the static drivers consume static power only when the data signal is high (and the enable signal is asserted if there is one). There is no dynamic power consumption (doesn't change with every clock cycle).

Referring to FIG. 9, a quasi-static interconnect system 140 illustrates quasi-static drivers 142A and 142B for bits 0 and 1 of a multiple bit signal, which are representative of other drivers and bits in system 140. Driver 142A includes nFET devices M5A, M6A, and M7A. The gate of device M5A is connected to the output of a NOR gate 144A. Driver 142B includes nFET devices M5B, M6B, and M7B. The gate of device M5B is connected to the output of a NOR gate 144B. Interconnect signals Q(0) and Q(1) on conductors 66A and 66B are the complement of Din(0) and Din(1) when the clock (Clk) is low (although the quasi-static drivers could be modified so that Q(0) and Q(1) follow the state of Din(0) and Din(1). Table 2 illustrates the operation of driver 142A, and is representative of the operation of driver 142B. Table 2 shows the state of the output of NOR gate 144A and the interconnect signal Q(0) as a function of the Clk and Din(0) inputs.

Clk	Din(0)	(Clk + Din(0))'	Q(0)
0	0	1	Vdd - Vt
0	1	0	Vgnd
1	0	0	Vgnd
1	1	0	Vgnd

Table 2

The Miller Coupling Factor (MCF) describes a phenomenon wherein the capacitance of an interconnect is increased when it has a changing voltage but its a neighboring interconnect(s) does/do not. The MCF may be doubled where the

B. Drivers

1. Drivers with Low Voltage Swing

In one embodiment, driver 54 may be a single-ended, tri-stated driver that uses an n-channel field effect transistor (nFET device) to provide a reduced voltage swing. In such a case, circuit 50 would be a mixed swing signal. Referring to Fig. 6, a driver 100 includes an nFET device M1, the gate of which receives the output of NOR gate 112. Data-in (Din) is inverted by an inverter 106. The output of inverter 106 is provided to the gate of an nFET device M2 and to one input to NOR gate 112. The enable signal (also called tri-state enable signal) is provided to the gate of an nFET device M3 and is inverted by an inverter 108, the output of which is provided as another input to NOR gate 112. The output of NOR gate 112 can be written as (En* + Din*)*. The operation of driver 100 can be illustrated through Table 1, below.

Enable	Din	(En* + Din*)*	M1	M2	M3	Q
0	0	0	OFF	ON	OFF	Tri state
0	1	0	OFF	OFF	OFF	Tri state
1	0	0	OFF	ON	ON	Vgnd
1	1	1	ON	OFF	ON	Vdd - Vt

Table 1

According to Table 1, if the Enable signal is unasserted (low), both M1 and M3 are OFF so that conductor 66 is in a tri-state high impedance condition regardless of the state of Din. When the Enable signal is unasserted, driver 100 is tri-stated, enabling other drivers connected to the same line to drive during the same clock phase. If enable is asserted (high), Q follows Din. However, because device M1 is an nFET device rather than a p-channel FET (pFET) device, nFET device M1 can pull signal Q up to only Vdd - Vt, which Vt is the threshold voltage of device M1. Note that in some embodiments, except for unintentional parameter variations, each nFET transistor in driver 100 and perhaps also receiver 58 may have the same threshold voltage. Alternatively, M1 may have a different threshold voltage through engineering or a voltage technique such as providing a forward body bias, described below. NFET device M1 is referred to as a source follower transistor because its source (at conductor 66) follows the input signal at the gate of M1.

Advantages of driver 100 include that because it is single ended, less space is used and less power is consumed than prior art fully differential techniques which uses

two interconnects. Less power is also used because of the lower voltage swing (i.e., Vdd - Vt, rather than Vdd) when compared to a full swing driver. The dynamic power reduction may be linear as Vdd - Vt is reduced from Vdd. An nFET device has roughly 2 to 2 ½ times the transconductance of a pFET device for the same size. Therefore, for the same size, an nFET device M1 pulls up faster than would a pFET device. Alternatively, nFET device M1 can be made smaller and trade off some switching speed. Driver 100 switches from high to low faster than do full swing drivers, because it does not have as far to go before reaching a trip point. However, this leads to lower noise immunity because high voltage signals (Vdd - Vt) are closer to the switching point Vdd/2. Accordingly, it is valuable to use a receiver 58 that has hysteresis such that interconnect signal Q has to go considerably below the trip point for a high to low transition. Such receivers are described below.

The reduced voltage swing across the load may result in a nearly linear reduction in driver delay compared to full-swing operation. This delay improvement may be achieved without a loss in the driver transistors' on-drive voltage (Vgs). Prior static CMOS-based low swing drivers for datapath interconnects suffer from a linear reduction in on-drive voltage with reducing voltage swings and hence offer much lesser delay improvement. The present approach enables considerable down-sizing of the driver transistors for a target delay constraint, leading to further power savings as well as layout area savings. Alternately, repeaterless interconnects can be driven for much longer distances on-chip than prior art approaches.

Because the driver is static (the interconnect state is switched only with a data transition), interconnect dynamic power may drop linearly with reducing interconnect switching activity. This represents a substantial savings in power compared to other dynamic prior art approaches, because such schemes precharge and evaluate the bus every cycle independent of input data activity, contributing to a large dynamic power loss at low input data activities.

Driver 100 may share the power and ground rails (Vdd and Vgnd) with peripheral circuitry (operating at CMOS levels, Vdd and Vgnd). Thus, no additional power supply rails (and associated circuitry) are needed. As compared to some prior art CMOS based low swing drivers, this provides a significant reduction in layout size.

between Vgnd and Q-High. Depending on the details of driver 54, Q-High is equal to or less than Vdd. Depending on the details of driver 54, Q follows signal Data-In or is its complement. Receiver 58 receives interconnect signal Q and provides a signal Data-Out (Dout), which has a swing between Vgnd and Vdd and follows signal Data-In or is its complement. Receiver 58 may also provide a Dout* signal which is the complement or inverse of Dout. R and C are the inherent resistance and capacitance of interconnect 66. Because of R, the voltage of signal Q will be reduced between driver 54 and receiver 58. In some embodiments, the amount of the reduction is negligible. Where that reduction is not negligible, there may be some decrease in noise immunity. However, the noise immunity may be improved by a hysteretic receiver described below.

A single ended driver is one that provides an interconnect signal on a single interconnect rather than also providing a complementary signal on a parallel interconnect as in prior art system 10 in FIG. 1. A single ended receiver is one that receives an interconnect signal on a single interconnect rather than two interconnects as in prior art system 10 in FIG. 1. A single ended signal is one where the information is conveyed in a single signal rather than through a signal and its complement in parallel. A single ended interconnect system is one with a single ended driver and single ended receiver.

Referring to FIG. 3, single ended interconnect system 70 is like system 50 in FIG. 2, except that a driver 74 of system 70 does not receive an enable signal and driver 54 of system 50 does. In the case of tri-stated drivers, multiple drivers can drive the same interconnect (with only one driver's tri-state enable signal asserted during a given clock phase). This can significantly improve interconnect routing channel density between and within the datapath FUBs for a given bus bandwidth.

In many implementations, different bits of a multi-bit signal are conveyed in parallel interconnects of single ended interconnect systems such as in FIG. 2 and 3. For example, FIG. 4 illustrates bit 0 and bit 1 of a multi-bit signal. Bit 0 is represented as Din(0) received by driver 54A, Q(0) on interconnect 66A, and Dout(0) at the output of receiver 58A. Bit 1 is represented as Din(1) received by driver 54B, Q(1) on interconnect 66B, and Dout(1) at the output of receiver 58B.

FIG. 5 illustrates two bits of a pseudo-differential interconnect system 90. Bit 0 is represented as Din(0), Q(0) on interconnect 66A, and Dout(0) at the output of fully differential receiver 92A. Bit 1 is represented as Din(1), Q(1) on interconnect 66B, and Dout(1) at the output of fully differential receiver 92B. Interconnects 66A and 66B are referred to as bit interconnects because they carry bit signals, even if at a reduced swing. Din(0) and Din(1) swing between 0 and Vdd. Q(0) and Q(1) swing between 0 and Qhigh. Depending on the particular implementation of drivers 54A and 54B, Qhigh may be equal to or less than Vdd. System 90 illustrates optional inverters 94A and 94B which invert Din(0) and Din(1) before they are received by drivers 54A and 54B, respectively. Inverters 94A and 94B may be used as drivers to increase the voltage of Din(0) and Din(1). Depending on the implementation, Q(0) and Q(1) follow or are the complement of Din(0) and Din(1), respectively. Depending on the implementation, Dout(0) and Dout(1) follow or are the complement of Q(0) and Q(1), respectively.

System 90 includes a reference interconnect 96 which carries a signal Vref. In some embodiments, Vref = Qhigh/2. In some embodiments, there is one reference interconnect for every 8 to 16 bit interconnects, of which interconnects 66A and 66B are examples. (Other ratios of references to interconnects may be used.) Accordingly, in system 90, the interconnect area penalty is substantially lower than in the prior art fully-differential scheme, while achieving the high common mode noise rejection advantage they enjoy. In some embodiments, when Vref = Qhigh/2 and Vref is set to a fixed DC bias voltage midway between the interconnect signal swing. Fully-differential receivers 92A and 92B receive signals Q(0) and Q(1), which may be reduced swing signals, and the reference voltage and deliver full-swing outputs Dout(0) and Dout(1). Because the reference interconnect is set to a fixed voltage (i.e., it does not transition), the dynamic power reduction achieved due to the lowered interconnect signal swing is retained, unlike a prior art fully-differential interconnect system wherein the switched capacitance is doubled.

The following sections provide examples of drivers 54 and 74, and receiver 58. As described below, in some embodiments, a prior art receiver (such as an inverter or two inverters in series) may be used.

FIG. 1 is a schematic representation of a prior art differential interconnect system including a differential driver, differential interconnects, and a differential receiver.

FIG. 2 is a schematic representation of a single ended interconnect system including single ended driver, an interconnect, and a single ended receiver according to some embodiments of the invention.

FIG. 3 is a schematic representation of a single ended interconnect system including single ended driver, interconnect, and receiver according to some embodiments of the invention.

FIG. 4 illustrates two single ended drivers, interconnects, and receivers in parallel.

FIG. 5 is a schematic representation of a pseudo-differential system including a single ended drivers, interconnects, and differential receivers according to some embodiments of the invention.

FIG. 6 is a schematic representation of a single ended driver according to some embodiments of the invention.

FIG. 7 is a schematic representation of a single ended driver according to some embodiments of the invention.

FIG. 8 is a schematic representation of a single ended driver according to some embodiments of the invention.

FIG. 9 is a schematic representation of a quasi-static interconnect system according to some embodiments of the invention.

FIG. 10 illustrates a p-boosted version of one of the drivers of the system of FIG. 9.

FIG. 11 is a schematic representation of a receiver according to some embodiments of the invention.

FIG. 12 is a schematic representation of a receiver according to some embodiments of the invention.

FIG. 13 is a graph illustrating hysteretic features of the receivers of FIGS. 11 and 12.

FIG. 14 is a schematic representation of a dual rail driver according to some embodiments of the invention.

FIG. 15 is a schematic representation of a single ended driver according to some embodiments of the invention.

FIG. 16 is a schematic representation of a single ended driver according to some embodiments of the invention.

FIG. 17 is a schematic representation of a bidirectional interconnect system.

FIG. 18 is a schematic representation of an enabled receiver for use in the system of FIG. 17.

FIG. 19 is a schematic representation of a receiver, for use in the system of FIG. 17, connected to logic which receives an enable input signal.

Detailed Description

A. System Overview

Referring to FIG. 2, a single ended interconnect system 50 includes a single ended driver 54 and a single ended receiver 58 connected through a single ended interconnect 66. Interconnect 66 may be a relatively long point-to-point on-chip datapath interconnect such as may be included in a microprocessor, digital signal processor, memory chip, or other integrated circuit chip, or be used between chips. Driver 54 receives a single ended Data-In (Din) signal, having a swing between Vgnd and Vdd, and converts it to a single ended interconnect signal Q, having a swing

8. An interconnect system comprising:

interconnects:

single ended drivers receiving respective data-in signals and an enable signal and wherein the drivers transmit interconnect signals on the interconnects when the enable signal is asserted; and

single ended hysteretic receivers connected to respective ones of the interconnects.

9. The system of claim 8, wherein the single ended drivers are a first group of drivers, the single ended hysteretic receivers are a first group of revivers, and the interconnect signals are a first group of interconnect signals, and wherein the system is a bidirectional signaling interconnect system including a second group of single ended drivers and a second group of single ended hysteretic receivers coupled to the interconnects, and wherein the second group of drivers transmits a second group of interconnect signals on the interconnect to the second receiver in an opposite direction than the first group of drivers transmits the interconnect signals to the first group of receivers.

10. The system of claim 8, wherein the receiver includes pull up transistors cross-coupled between nodes and a transistor connected to one of the nodes that accelerates the fall of one of the nodes and after a low to high transition of an input signal, holds the node to a low voltage unless the input signal goes below a reverse trip point which is lower than a forward trip point.

11. The system of claim 8, wherein the receiver includes a riding transistor involving no static power consumption.

12. The system of claim 8, wherein the drivers include an nFET source follower device that pull ups an interconnect signal to a first voltage value and a p-booster pFET device pulls the interconnect signal to a power supply voltage.

13. The system of claim 8, wherein the driver transmits an interconnect signal that has a high voltage equal to a power supply voltage minus a threshold voltage of an nFET device and wherein the system further includes body bias voltage circuitry to control the threshold voltage of the nFET device.

14. An interconnect system comprising:

interconnects;

quasi-static drivers to transmit interconnect signals on the interconnects, the quasi-static drivers receiver a clock signal and respective data-in signals, and wherein the interconnect signals are pre-discharge when the clock signal changes from a first to a second state, and wherein when the clock signal is in the first state, the interconnect signals are related to the data-in signals; and

receivers connected to respective ones of the interconnects.

15. The system of claim 14, wherein the first state is a high voltage and the second state is a low voltage.

16. The system of claim 14, wherein the interconnect signals are related to the data-in signals in an inverse relationship.

17. The system of claim 14, wherein the drivers include an nFET source follower device that pull ups an interconnect signal to a first voltage value and a p-booster pFET device pulls the interconnect signal to a power supply voltage.

18. The system of claim 14, wherein the driver transmits an interconnect signal that has a high voltage equal to a power supply voltage minus a threshold voltage of an nFET device and wherein the system further includes body bias voltage circuitry to control the threshold voltage of the nFET device.

19. An pseudo differential interconnect system comprising:

interconnects;

a reference conductor;

single ended drivers providing interconnect signals to the respective ones of the interconnects; and

differential receivers each connected to the reference conductor and one of the interconnects.

20. An interconnect system, comprising:

an interconnect carrying an interconnect signal;

a single ended receiver connected to the interconnect; and

a dual rail driver receiving a clock signal and a data signal, and when the clock signal is in a first state, the interconnect signal is precharged to low and when the clock

signal is in a second state, the interconnect signal is a function of a state of the data signal without contention between pull up and pull down transistors.

21. A hysteretic circuit comprising:

an input conductor carrying an input signal; and

cascode voltage switched gate with an additional transistor that has a hysteretic effect by keeping a node at a low voltage unless the input signal goes below a reverse trip point that is lower than a forward going trip point.

22. The circuit of claim 21, wherein the node is a second node, and wherein the cascode voltage switched gate includes:

first and second pull up transistors; and

first and second pull down transistors, wherein the first pull up transistor and the first pull down transistor are coupled through a first node, and the second pull up transistor and the second and third pull down transistors are coupled through the second node, and wherein a gate of the second pull down transistor is coupled to the input conductor, and a gate of the third pull down transistor is connected to the first node.

23. The circuit of claim 21, wherein the additional transistor is a pull down transistor.

24. The circuit of claim 21, wherein the first transistor is a riding transistor involving no static power consumption.

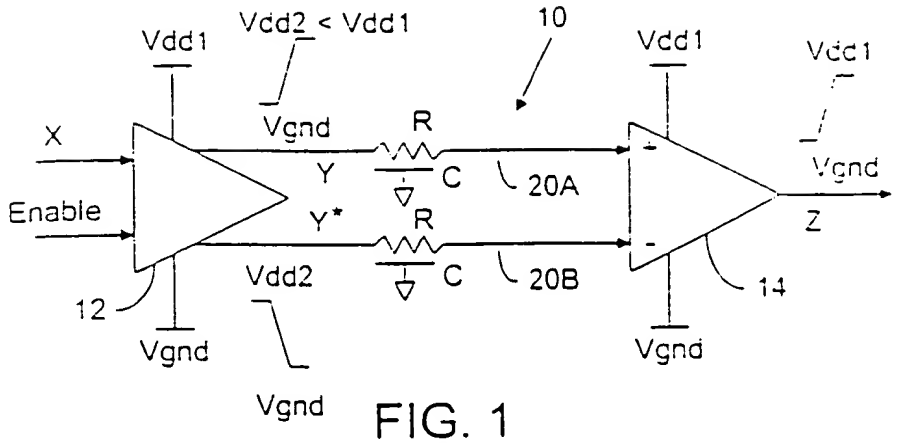

FIG. 1
(PRIOR ART)

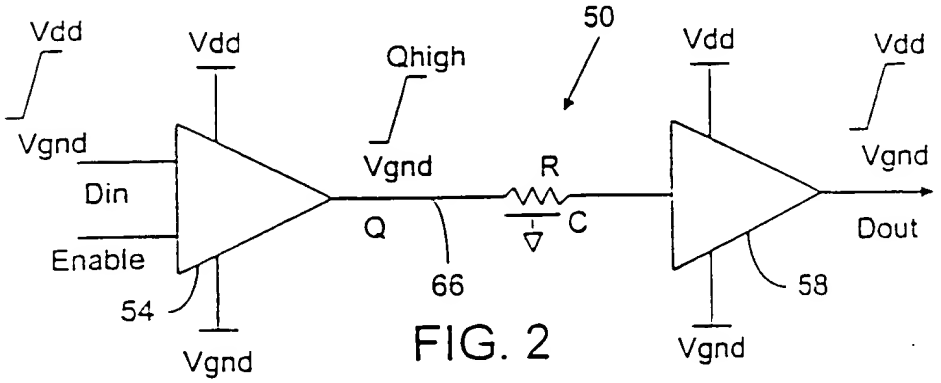

FIG. 2

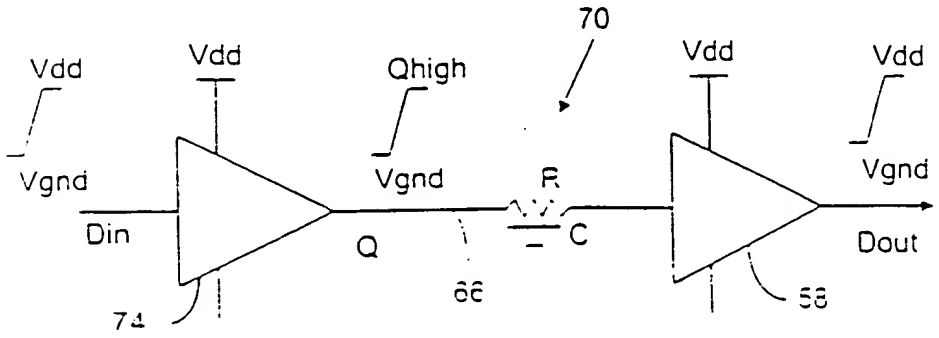

FIG. 3

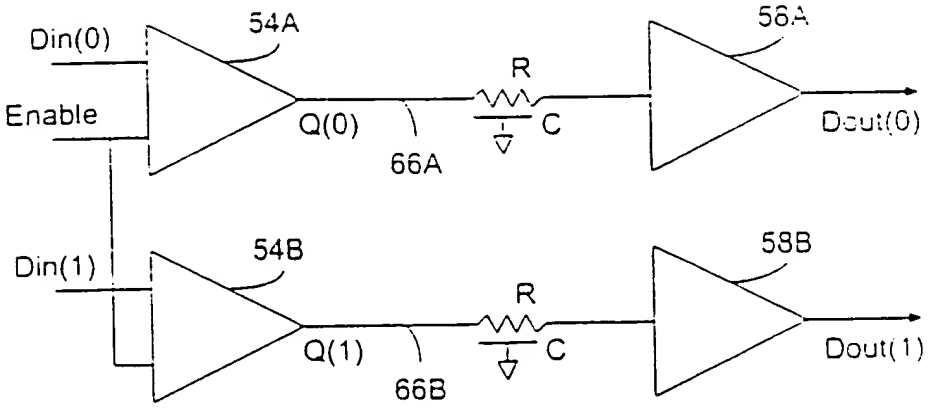
Din(0)
54A
Enable
Q(0)
66A
R
C
58A
Dout(0)
Din(1)
54B
Q(1)
66B
R
C
58B
Dout(1)

FIG. 4

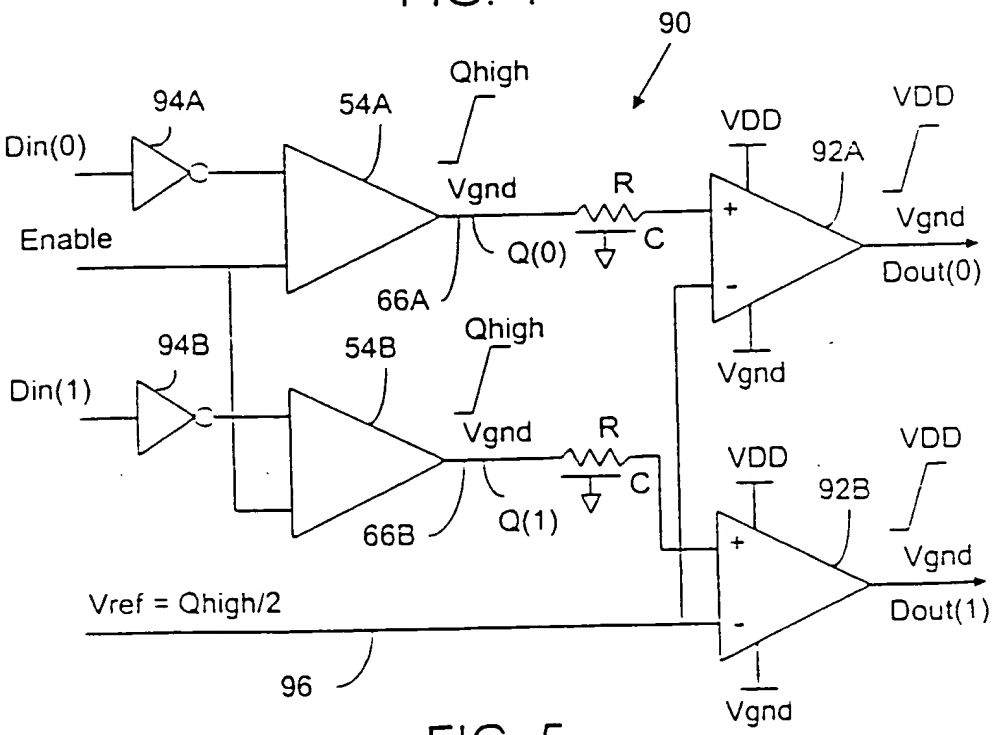
90
Qhigh
94A
54A
Din(0)
Vgnd
R
VDD
92A
VDD
Enable
Q(0)
C
Vgnd
Dout(0)
66A
Vgnd
94B
54B
Qhigh
Din(1)
Vgnd
R
VDD
VDD
C
92B
Q(1)
66B
Vgnd
Vref = Qhigh/2
Dout(1)
96
Vgnd

FIG. 5

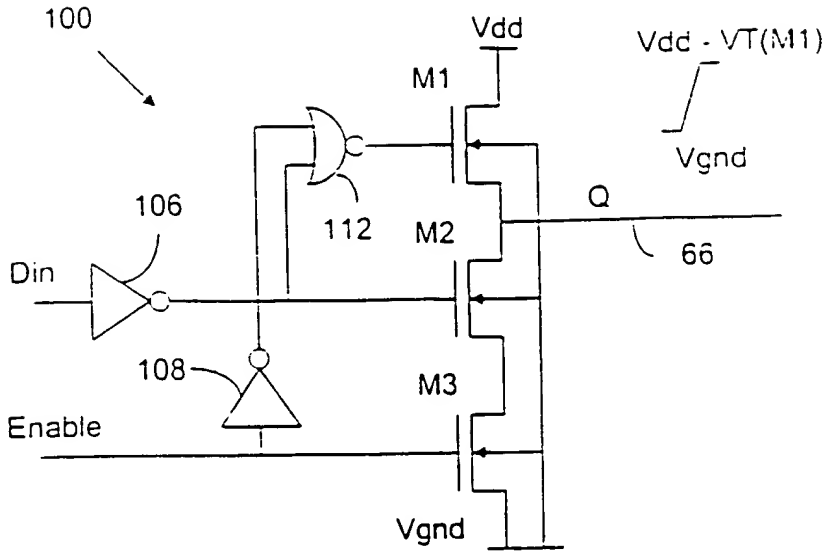
100
Vdd
Vdd - VT(M1)
M1
Vgnd
106
112
M2
Q
66
Din
108
M3
Enable
Vgnd

FIG. 6

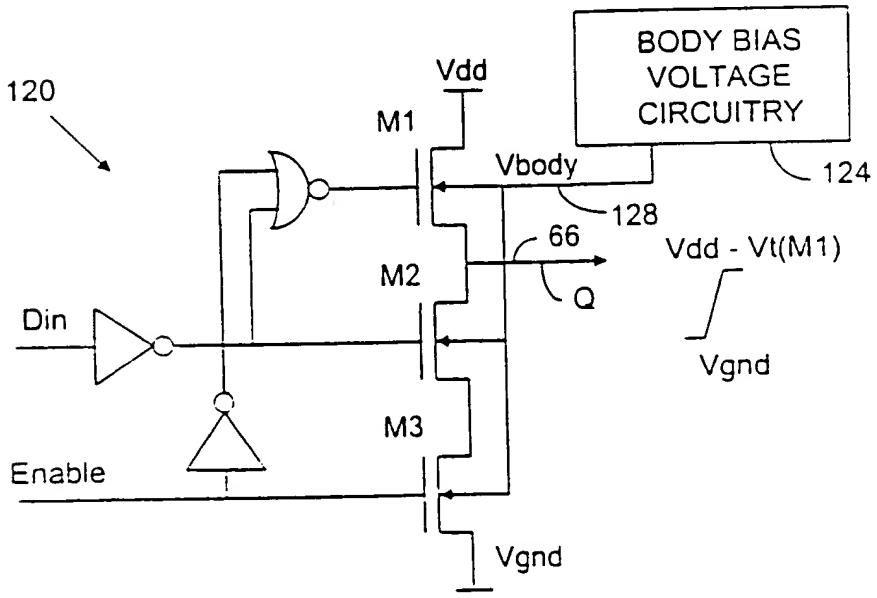
BODY BIAS
VOLTAGE
CIRCUITRY
124
120
Vdd
M1
Vbody
128
66
Vdd - Vt(M1)
M2
Q
Din
Vgnd
M3
Enable
Vgnd

FIG. 7

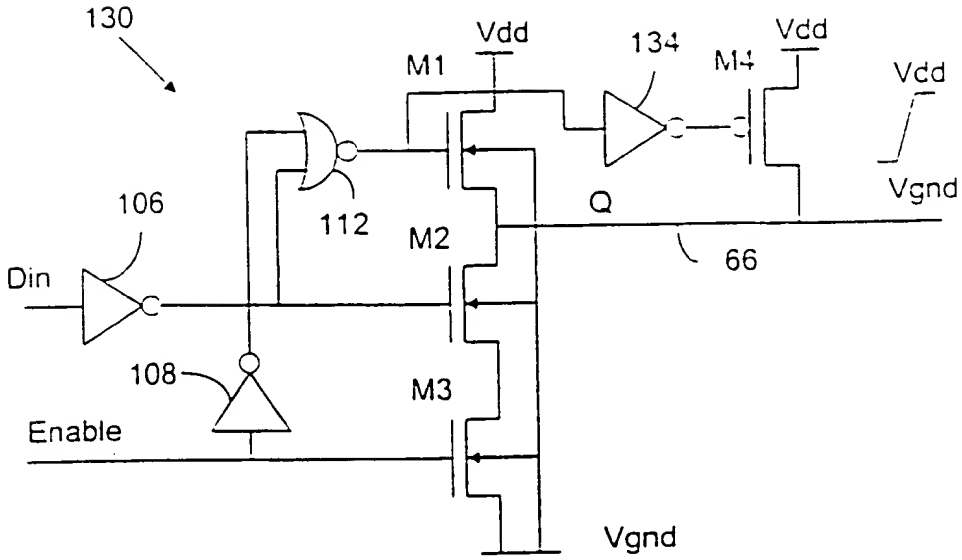
130
Vdd
M1
134
M4
Vdd
Vdd
Vgnd
106
112
M2
Q
66
Din
108
M3
Enable
Vgnd

FIG. 8

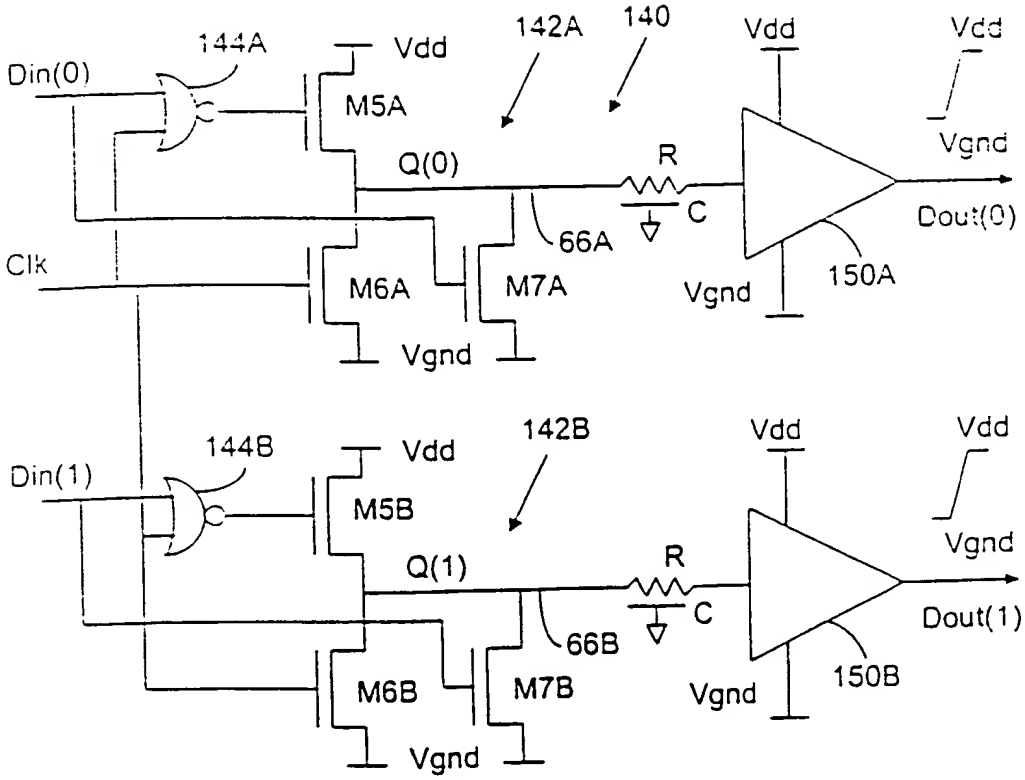
Din(0)
144A
Vdd
M5A
142A
140
Vdd
Vdd
Vgnd
Q(0)
R
C
Dout(0)
66A
Clk
M6A
M7A
Vgnd
150A
Vgnd
Din(1)
144B
Vdd
M5B
142B
Vdd
Vdd
Vgnd
Q(1)
R
C
Dout(1)
66B
M6B
M7B
Vgnd
150B
Vgnd

FIG. 9

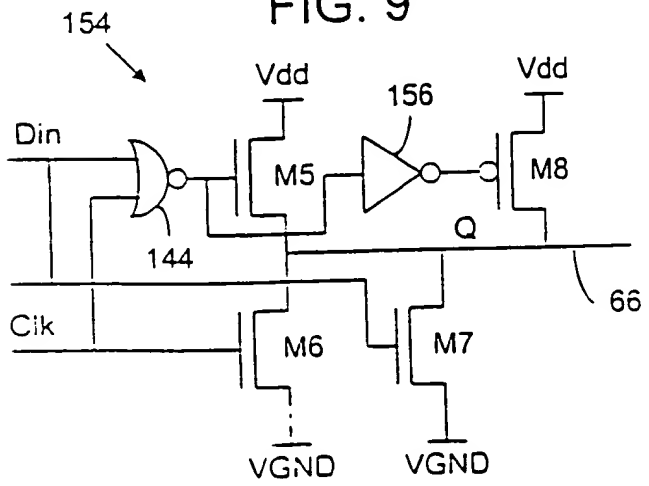
154
Vdd
156
Vdd
Din
M5
M8
Q
144
66
Clk
M6
M7
VGND
VGND

FIG. 10

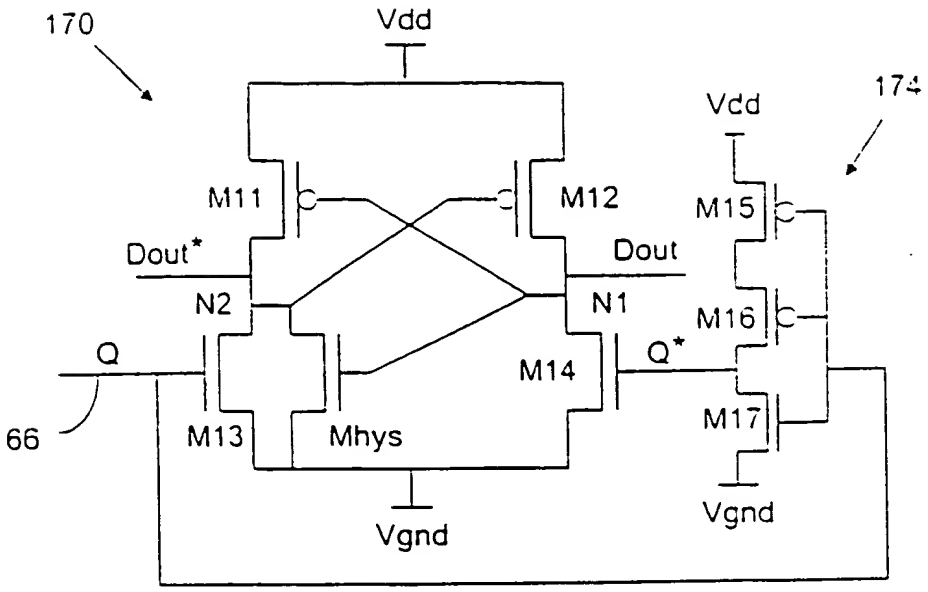
170
Vdd
Vdd
174
M11
M12
M15
Dout*
Dout
N2
N1
M16
Q
Q*
M14
66
M13
Mhys
M17
Vgnd
Vgnd

FIG. 11

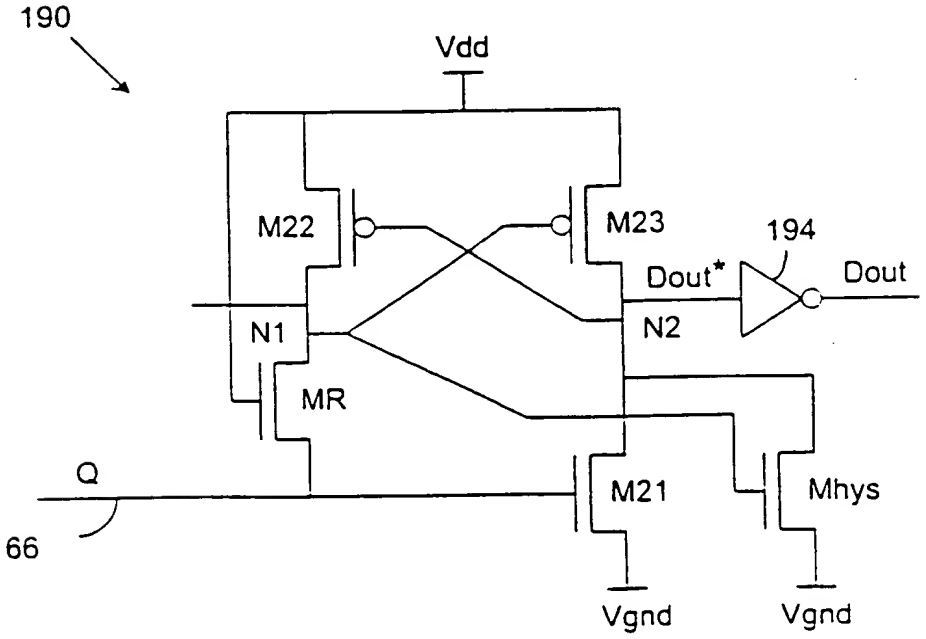
190
Vdd
M22
M23
194
Dout*
Dout
N1
N2
MR
Q
M21
Mhys
66
Vgnd
Vgnd

FIG. 12

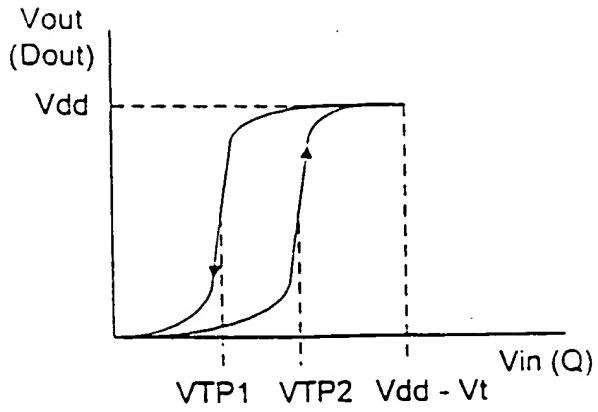
Vout
(Dout)
Vdd
Vin (Q)
VTP1
VTP2
Vdd - Vt

FIG. 13

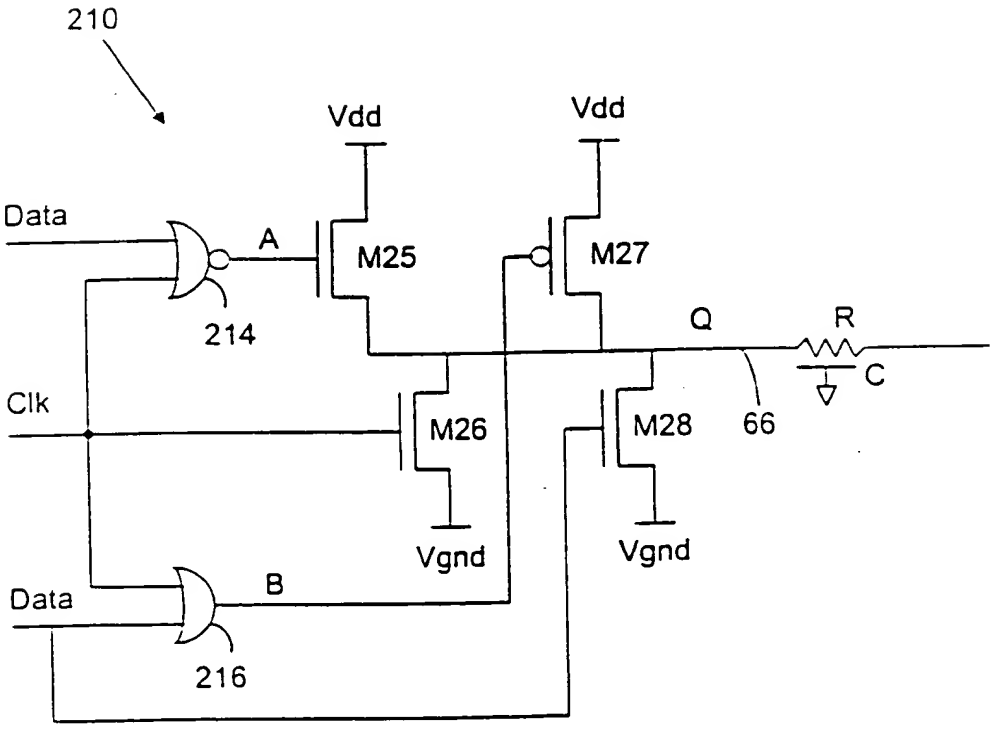
210
Vdd
Vdd
Data
A
M25
M27
214
Q
R
C
Clk
M26
M28
66
Vgnd
Vgnd
Data
B
216

FIG. 14

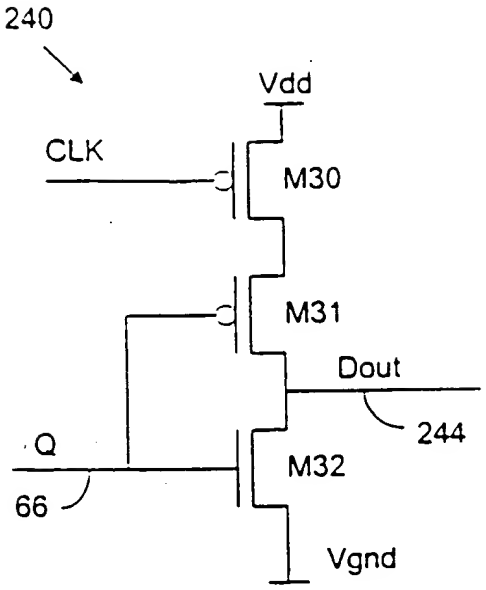
240
Vdd
CLK
M30
M31
Dout
244
Q
M32
66
Vgnd

FIG. 15

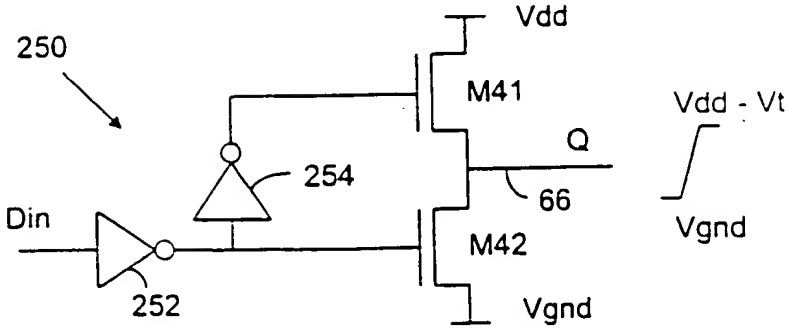
250
Vdd
M41
Vdd - Vt
Q
254
66
Din
M42
Vgnd
252
Vgnd

FIG. 16

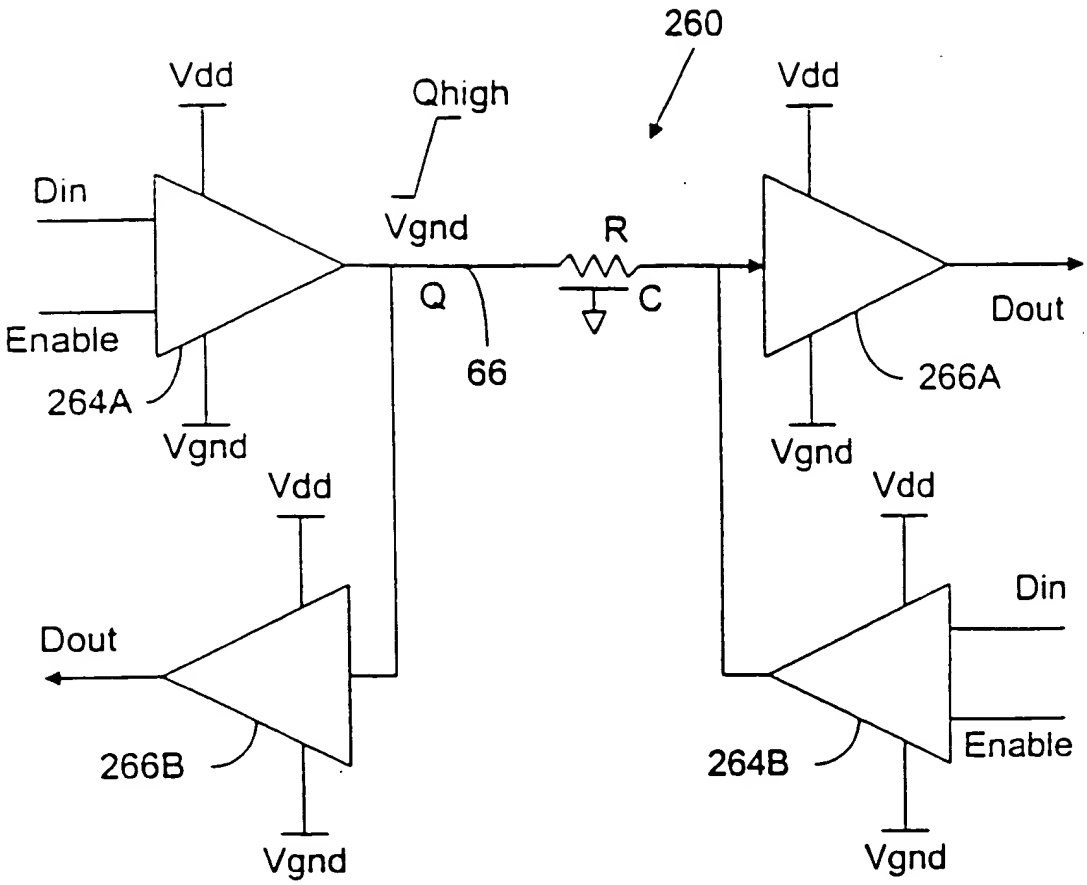

FIG. 17

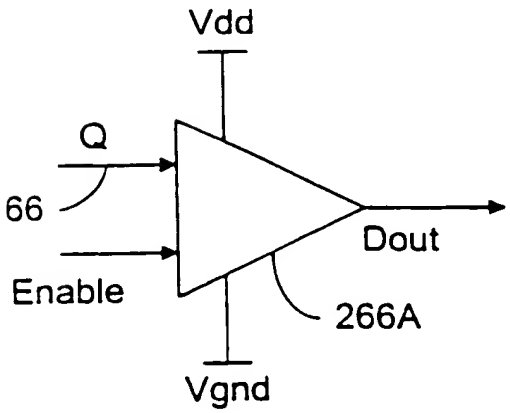

FIG. 18

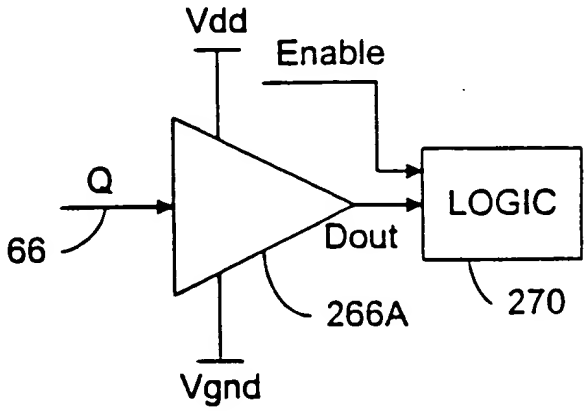

FIG. 19

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/20674

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H03K 3/12, 3/286
US CL : 327/205, 206

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 327/63, 65, 66, 67, 70, 78, 70, 80, 81, 205, 206, 534, 535
326/28

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

U.S. PTO APS East
search terms: (hystere$ or schmitt) , driver, cross

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,559,461 A (Yamashina et al.) 24 SEPTEMBER 1996 (29.09.96), figure 17	1
X --- Y	Low-Swing Interconnect Interface Circuits Proceeding of Int'l Symp. Om Low Power Electronics and Design, 10 August 1998 (10.08.98), pp 161-66, figure 6	1, 3, 4, 21, 23, 24 --- 2, 5-16, 20
X	US 5,594,361 A (Campbell) 14 January 1997 (14.01.97), figure 5	21-23
Y	US 5,086,427 A (Whittaker et al.) 04 FEBRUARY 1992 (04.02.92), figure 1	2, 9

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
08 DECEMBER 1999	14 FEB 2000

Name and mailing address of the ISA/US	Authorized officer
Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231	ANH- QUAN TRA
Facsimile No. (703) 305-3230	Telephone No. (703) 308-0[illegible]

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/20674

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X -- Y -- A	US 5,644,255 A (Taylor) 1 JULY 1997 (01.07.97), figure 4	19 --- 5, 6, 12 --- 17, 18
Y, T	US 5,986,473 A (Krishnamurthy et al.) 16 NOVEMBER 1999 (16.11.99), figure 2	7-13
Y, T	US 5,994,918 A (Mehra) 30 NOVEMBER 1999 (30.11.99) Figure 2	14-16, 20

Form PCT/ISA/210 (continuation of second sheet)(July 1992)*

PATENT COOPERATION TREATY

PCT

From the INTERNATIONAL BUREAU

NOTICE INFORMING THE APPLICANT OF THE COMMUNICATION OF THE INTERNATIONAL APPLICATION TO THE DESIGNATED OFFICES

(PCT Rule 47.1(c), first sentence)

To:
MILLIKEN, Darren, J.
Blakely, Sokoloff, Taylor & Zafman LLP
7th floor
12400 Wilshire Boulevard
Los Angeles, CA 90025
ETATS-UNIS D'AMERIQUE

Date of mailing (day/month/year)	
30 March 2000 (30.03.00)	
Applicant's or agent's file reference	**IMPORTANT NOTICE**
42390.P6182	

International application No.	International filing date (day/month/year)	Priority date (day/month/year)
PCT/US99/20674	10 September 1999 (10.09.99)	18 September 1998 (18.09.98)

Applicant
INTEL CORPORATION et al

1. Notice is hereby given that the International Bureau has communicated, as provided in Article 20, the international application to the following designated Offices on the date indicated above as the date of mailing of this Notice:
   AU,CN,JP,KP,KR,US

   In accordance with Rule 47.1(c), third sentence, those Offices will accept the present Notice as conclusive evidence that the communication of the international application has duly taken place on the date of mailing indicated above and no copy of the international application is required to be furnished by the applicant to the designated Office(s).

2. The following designated Offices have waived the requirement for such a communication at this time:
   AE,AL,AM,AP,AT,AZ,BA,BB,BG,BR,BY,CA,CH,CU,CZ,DE,DK,EA,EE,EP,ES,FI,GB,GD,GE,GH,GM,HR,HU,ID,IL,IN,IS,KE,KG,KZ,LC,LK,LR,LS,LT,LU,LV,MD,MG,MK,MN,MW,MX,NO,NZ,OA,PL,PT,RO,RU,SD,SE,SG,SI,SK,SL,TJ,TM,TR,TT,UA,UG,UZ,VN,YU,ZA,ZW
   The communication will be made to those Offices only upon their request. Furthermore, those Offices do not require the applicant to furnish a copy of the international application (Rule 49.1(a-bis)).

3. Enclosed with this Notice is a copy of the international application as published by the International Bureau on
   30 March 2000 (30.03.00) under No. WO 00/18009

REMINDER REGARDING CHAPTER II (Article 31(2)(a) and Rule 54.2)

If the applicant wishes to postpone entry into the national phase until 30 months (or later in some Offices) from the priority date, a **demand for international preliminary examination** must be filed with the competent International Preliminary Examining Authority before the expiration of 19 months from the priority date.

It is the applicant's sole responsibility to monitor the 19-month time limit.

Note that only an applicant who is a national or resident of a PCT Contracting State which is bound by Chapter II has the right to file a demand for international preliminary examination.

REMINDER REGARDING ENTRY INTO THE NATIONAL PHASE (Article 22 or 39(1))

If the applicant wishes to proceed with the international application in the **national phase**, he must, within 20 months or 30 months, or later in some Offices, perform the acts referred to therein before each designated or elected Office.

For further important information on the time limits and acts to be performed for entering the national phase, see the Annex to Form PCT/IB/301 (Notification of Receipt of Record Copy) and Volume II of the PCT Applicant's Guide.

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

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